DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-10, 17-18, 21-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites a "buffer storing indications of events" in line 2, "said apparatus for transferring interrupts from the peripheral device to a host computer" in lines 9-10, "moving the contents of the buffer to the payload portion of the control data block, and sending the control data block to the host computer system" in lines 18-19. The recitations suggest that indications of events are stored in the buffer and that the indications of events (the contents of the buffer) are moved to a payload portion of the control data block and sending the control data block to the host computer system. The recitations also suggest that only interrupts from the indications of events (i.e. not the indications of events) are transferred from the peripheral device to the host computer system. It appears that the specification only discloses transferring all indications of

events in the control block to the host computer.

4. Claims 11-16, 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

It appears that there is no support for "moving the contents of the buffer to the corresponding fields of the payload portion" - as page 38, lines 25-26 merely discloses "when preset conditions are met, an Interrupt Control Block (ICB) 1680 is generated by the ISOC 120 from the information stored in the interrupt FIFO 1660".

5. Claims 13-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 13 recites "at least a predetermined plurality of indications is stored in the buffer". Claim 14 recites "at least one indication is stored in the buffer". Claim 15 recites "a count indicative of the number of indications included in the payload portion". Claim 1 suggests storing only interrupts in the buffer and does not suggest storing indications other than interrupts in the buffer. The claims suggest that interrupts and indications are two different entities, while the specification only discloses only one

entity being stored in the buffer and the count being indicative of only one entity.

6. Claims 10, 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The examiner cannot find support for the limitations of the claims. In particular, it is not clear what constitute the claimed apparatus, the claimed host processing system, the claimed memory of the host processing system, the claimed data processing system, the claimed host computer, and the claimed memory of the host computer system.

Applicant is required to specifically point out where to find the support for the limitations of the claims in the specification, by page and line number - and in particular, applicant is required to map out each of the elements claimed with the teachings of the specification.

7. No art rejection was made to claims 1-16, 21-22 because the scope of the claims is ambiguous, and it is not possible for the examiner to apply prior art without making a great deal of speculation.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Raasch et al. (US 5,333,273).

10. As per claims 17, 19, Raasch teaches a computer program product (or article of manufacture) comprising a computer usable medium [138, FIG. 1] having computer readable program code means [BIOS: col. 5, lines 18-21] embodied therein for causing transfer of interrupts [col. 4, lines 66-68], the computer readable program code means in said computer program product (or article of manufacture) comprising computer readable program code means [BIOS: col. 5, lines 18-21] for causing a computer [100, FIG. 1] to effect the functions of the apparatus of claim 1 (or the method of claim 11) - as the BIOS would cause a computer to effect the functions of any apparatus, hence including functions of the apparatus of claim 1; and as the BIOS would cause a computer to effect the steps of any method, hence including the steps of the method of claim 11.

11. As per claim 18, Raasch teaches a computer program product comprising a computer usable medium [138, FIG. 1] having computer readable program code means [BIOS: col. 5, lines 18-21] embodied therein for causing data processing [col. 5, lines 18-31], the computer readable program code means in said computer program product comprising computer readable program code means [BIOS: col. 5, lines 18-21] for causing a computer [100, FIG. 1] to effect the functions of the apparatus of claim 10 - as

the BIOS would cause the computer to effect the functions of any apparatus, hence including the functions of the apparatus of claim 10.

12. As per claim 20, Raasch teaches a program storage device [138, FIG. 1] readable by machine [100, FIG. 1], tangibly embodying a program of instructions [BIOS: col. 5, lines 18-21] executable by the machine to perform method steps for transferring interrupts [col. 4, lines 66-68], said method steps comprising the steps of claim 11 (the BIOS would cause a computer to effect the steps of any method, hence including the steps of the method of claim 11).

Response to Arguments

13. Applicant's arguments filed February 19, 2008 have been fully considered but they are not persuasive.

A. With respect to the rejections of claims 1-10, 17-18, 21-22, applicant indicates that “a buffer storing indications of events” is recited on page 2, line 4. Page 2, line 4, however, recites “a buffer for storing indications of **interrupts**”. Note that “indications of interrupts” and “indications of events” do not have the same meaning.

B. With respect to the rejections of claims 11-16, 19-20, applicant indicates that "moving the contents of the buffer to the corresponding fields of the payload portion" is recited on page 44, line 10. While the recitation is found on page 44, line 10, the recitation is part of a claim that does not have antecedent basis in the specification – as page 38, lines 25-26 merely discloses "when preset conditions are met, an Interrupt Control Block (ICB) 1680 is generated by the ISOC 120 from the information stored in

the interrupt FIFO 1660".

C. With respect to the rejections of claims 13-15, applicant indicates the recitations are found on page 5, line 2; page 5, line 4; and page 5, line 7. The examiner found the recitations on page 5, lines 4-5; page 5, lines 6-7; and page 5, lines 9-10 instead. While the recitations can be found, the specification suggests storing only interrupts in the buffer and does not suggest storing indications in the buffer. The claims suggest that interrupts and indications are two different entities, while the specification only discloses only one entity being stored in the buffer and the count being indicative of only one entity (the one entity being interrupts).

D. With respect to the rejections of claims 10 and 22, applicant does not adequately provide support for the claimed elements requested by the examiner.

E. With respect to the art rejections of claims 17-20, applicant argues that Raasch is not concerned with or teach indications of events or a preset condition as in the claims. Raasch was not relied upon to teach indications of events or a preset condition, because **the claims do not require such limitations**. Applicant appears to misinterpret the rejections.

Claim 17 only requires a program code means for causing transfer of interrupts, and a program code means for causing a computer to **effect** all functions of the apparatus of claim 1. Claim 18 only requires a program code means for causing a computer to **effect** all functions of the apparatus of claim 10. Claim 19 only requires a program code means for causing transfer of interrupts, and a program code means for causing a computer to **effect** all steps of the method of claim 11. Claim 20 only

requires a program of instructions to **perform** method steps for transferring interrupts, the method steps comprising steps of the method steps of the method of claim 11.

Raasch teaches a BIOS and transfer of interrupts (col. 4, lines 66-68; col. 5, lines 16-21). **A BIOS would cause a computer to effect the functions of any apparatus (i.e. including the functions of applicant's apparatus), and because a BIOS would cause a computer to effect/perform the steps of any method (i.e. including the steps of applicant's methods)**.

14. In addition, to help the examiner better understand the scope of the claimed invention and further the prosecution, the examiner requests that applicant identify - by reference to labels in the drawings, and/or page and line numbers in the specification - the following elements and/or steps:

elements: apparatus, buffer, indications of interrupts, plurality of ports, peripheral device, host computer system, controller (in claim 1); communications device (in claims 8-9); data communications network interface (in claims 9-10); host processing system, data processing system (in claim 10)

steps: the apparatus transferring interrupts, moving the contents of the buffer to the payload portion of the control data block (claim 1); storing interrupts, moving the contents of the buffer to the corresponding fields of the payload portion (in claim 11).

In the interview dated June 16, 2008, applicant identifies the followings:

Apparatus is ISOC 120 [FIG. 17]

Buffer is FIFO 1660 [FIG. 17]

Interrupts are indications of events (i.e. "indications of interrupts" are therefore meaningless)

Plurality of ports can be logical or physical – but no identification of a plurality of ports for a peripheral device was made

Peripheral device is device 20 [FIG. 1]

Host computer system is any of Host 10 [FIG. 1], or Host 10 [FIG. 17]

Controller is inherent for generating control data block [1680, FIG. 17]

Communication device is network adapter 80 [FIG. 2]

Data communication network interface is network adapter 80 [FIG. 2]

Host processing system is CPU 50 [FIG. 1]

Data processing system is ISOC 120 [FIG. 2]

A memory in line 2 of claim 10 may not be memory 60 [FIG. 1, FIG. 17]

Data communication interface is network adapter 80 [FIG. 2]

Data communication network is network 30 [FIG. 1]

The above identifications cannot support the followings:

An apparatus [120, FIG. 17] moving the contents of the buffer [1660, FIG. 17] to the payload portion of the control data block, and sending the control data block to the host computing system [10, FIG. 17] via one port of the plurality of ports – as FIG. 17 shows sending the control data block [1680] to the host computing system through memory [60, FIG. 17], i.e. **not** through a port of the plurality of ports (of the peripheral device 20 – FIG. 1] – see lines 18-20 of claim 1.

A data communication network interface [80, FIG. 2] comprising the

communication device as claimed in claim 8 [i.e. communication device 80, FIG. 2] – see claim 9.

An apparatus [120, FIG. 17] comprising a host processing system [50, FIG. 1] having a memory [not identified]…forming a data processing system [120, FIG. 17] for controlling flow of interrupts from the data communication interface [80, FIG. 2] to the memory of the host processing system because FIG. 1, FIG. 2 and FIG. 17 do not show the apparatus 120 comprising CPU 50 – see claim 10.

The examiner is not quite sure what applicant intends to claim with the current claims. The examiner suggests that applicant maps the claims to the teachings of the disclosure, makes appropriate amendments, and requests an interview with the examiner to explain what is being claimed prior to filing a response to further prosecution of the application. Without understanding what applicant intends to claim, it is not possible for the examiner to properly examine the invention.

Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TANH Q. NGUYEN whose telephone number is (571)272-4154. The examiner can normally be reached on M-F (9:30AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TARIQ HAFIZ can be reached on (571)272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TANH Q. NGUYEN/
Primary Examiner, Art Unit 2182

TQN: July 5, 2008